IN THE CLAIMS

1. (Original) A method of producing a top gate thin-film transistor, comprising the steps of:

forming doped silicon source and drain regions on an insulating substrate;

subjecting the face of the substrate on which the source and drain regions are formed to plasma treatment to form a doped surface layer having impurity atoms diffused therein;

forming an amorphous silicon layer on the doped surface layer over at least the spacing between the source and drain regions;

forming an insulated gate structure over the amorphous silicon layer comprising a gate insulator and an upper gate conductor, the gate conductor being patterned to be narrower than the spacing between the source and drain regions;

laser annealing areas of the amorphous silicon layer not shielded by the gate conductor to form polysilicon portions having the impurities diffused therein.

2. (Original) A method as claimed in claim 1, additionally comprising the step of forming source and drain electrodes with which contact is made by the source and drain regions.

3. (Original) A method as claimed in claim 2, wherein the source and drain electrodes are formed on the insulating substrate before the formation of the source and drain regions, the source and drain regions at least partially overlying the source and drain electrodes.

4. (Original) A method as claimed in claim 2 or 3, wherein the source and drain electrodes comprise ITO or MoCr.

5. (Original) A top gate thin-film transistor comprising:

doped silicon source and drain regions defined from a first silicon layer over an insulating substrate;

second silicon layer overlying the first silicon layer and extending between the source and drain regions, source and drain portions of the second silicon layer which contact the source and drain regions comprising doped polysilicon and a channel portion of the second silicon layer between the source and drain portions, which is narrower than the spacing between the source and drain regions, comprising substantially undoped amorphous silicon; and

an insulated gate structure over the channel portion of the second silicon layer.

6. (Original) A transistor as claimed in claim 5, wherein the source and drain regions comprise doped polysilicon.

7. (Original) A transistor as claimed in claim 5 or 6, further comprising metallic source and drain electrodes which contact the source and drain regions.

8. (Original) A transistor as claimed in claim 7, wherein the source and drain regions overlie the source and drain electrodes.

9. (Original) A transistor as claimed in claim 7 or 8, wherein the source and drain electrodes comprise ITO or MoCr.

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